

TOSHIBA

**DISCONTINUATION NOTICE
TB62726AFG, TB62726AFGEL
TB62726ANG**

**THE FOLLOWING HAS BEEN
DISCONTINUED AS OF MAR 2009:**

**TB62726AFG, TB62726AFGEL
TB62726ANG**

**PLEASE SEE SUGGESTED
REPLACEMENT DRIVERS:
TCA62746AFGEL
TB62747AFGEL**

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TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB62726ANG, TB62726AFG

16-bit Constant-Current LED Driver with Operating Voltage of 3.3-V and 5-V

The TB62726A series are comprised of constant-current drivers designed for LEDs and LED displays. The output current value can be set using an external resistor.

As a result, all outputs will have virtually the same current levels.

This driver incorporates 16-bit constant-current outputs, a 16-bit shift register, a 16-bit latch and a 16-bit AND-gate circuit.

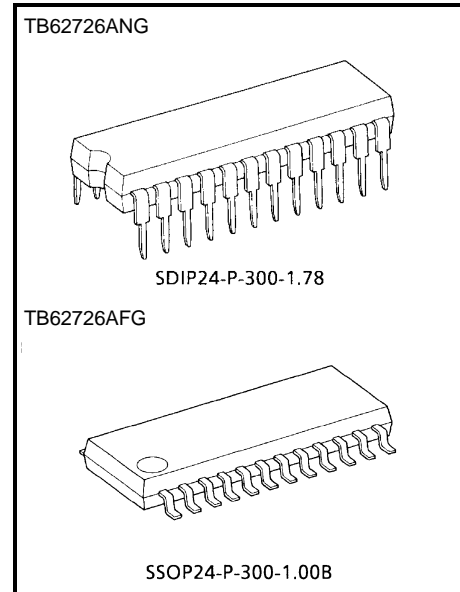
These drivers have been designed using the Bi-CMOS process.

This devices are a product for the Pb free.

Features

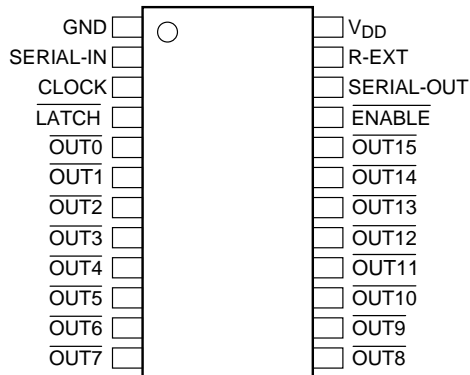
- Output current capability and number of outputs:
90 mA × 16 outputs
- Constant current range: 2 to 90 mA
- Application output voltage: 0.7 V (output current 2 to 80 mA)
0.4 V (output current 2 to 40 mA)
- For anode-common LEDs
- Input signal voltage level: 3.3-V and 5-V CMOS level (Schmitt trigger input)
- Power supply voltage range VDD = 3.0 to 5.5 V
- Maximum output terminal voltage: 17 V
- Serial and parallel data transfer rate: 20 MHz (max, cascade connection)
- Operating temperature range T_{opr} = -40 to 85°C
- Package: Type ANG: SDIP24-P-300-1.78
Type AFG: SSOP24-P-300-1.00B
- Current accuracy (All output ON)

Output Voltage	Current Accuracy		Output Current
	Between Bits	Between ICs	
≥ 0.4 V	±4%	±15%	2 to 5 mA
≥ 0.7 V		±12%	5 to 80 mA



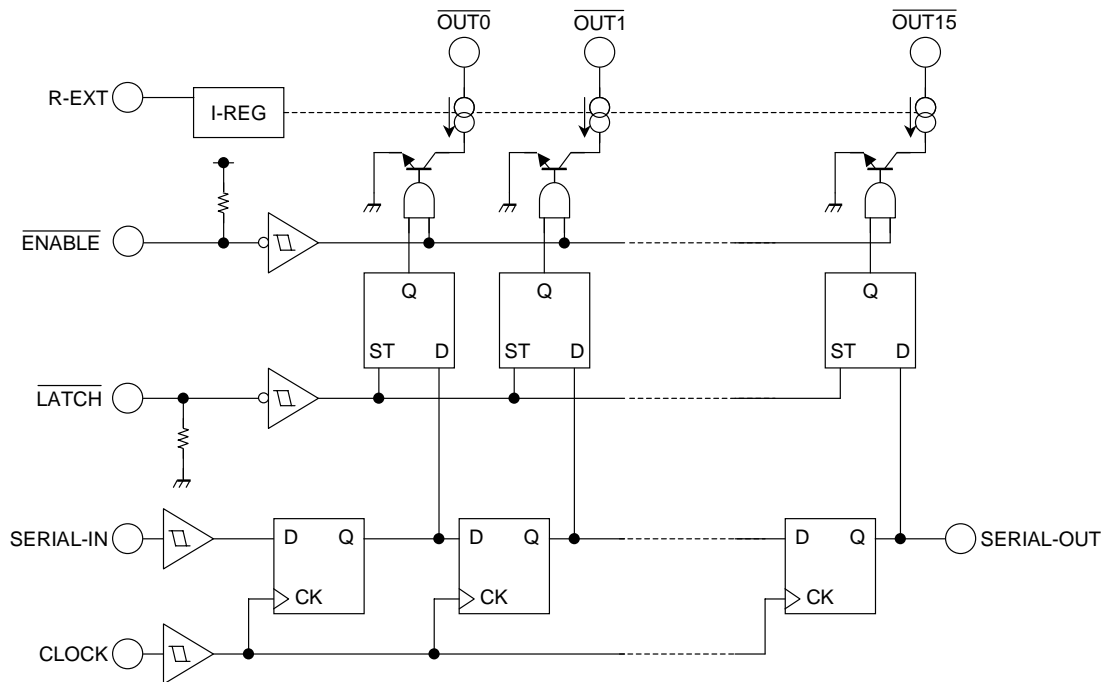
Weight
 SDIP24-P-300-1.78: 1.22 g (typ.)
 SSOP24-P-300-1.00B: 0.32 g (typ.)

Pin Assignment (top view)



Warnings: Short-circuiting an output terminal to GND or to the power supply terminal may broken the device.
Please take care when wiring the output terminals, the power supply terminal and the GND terminals.

Block Diagram



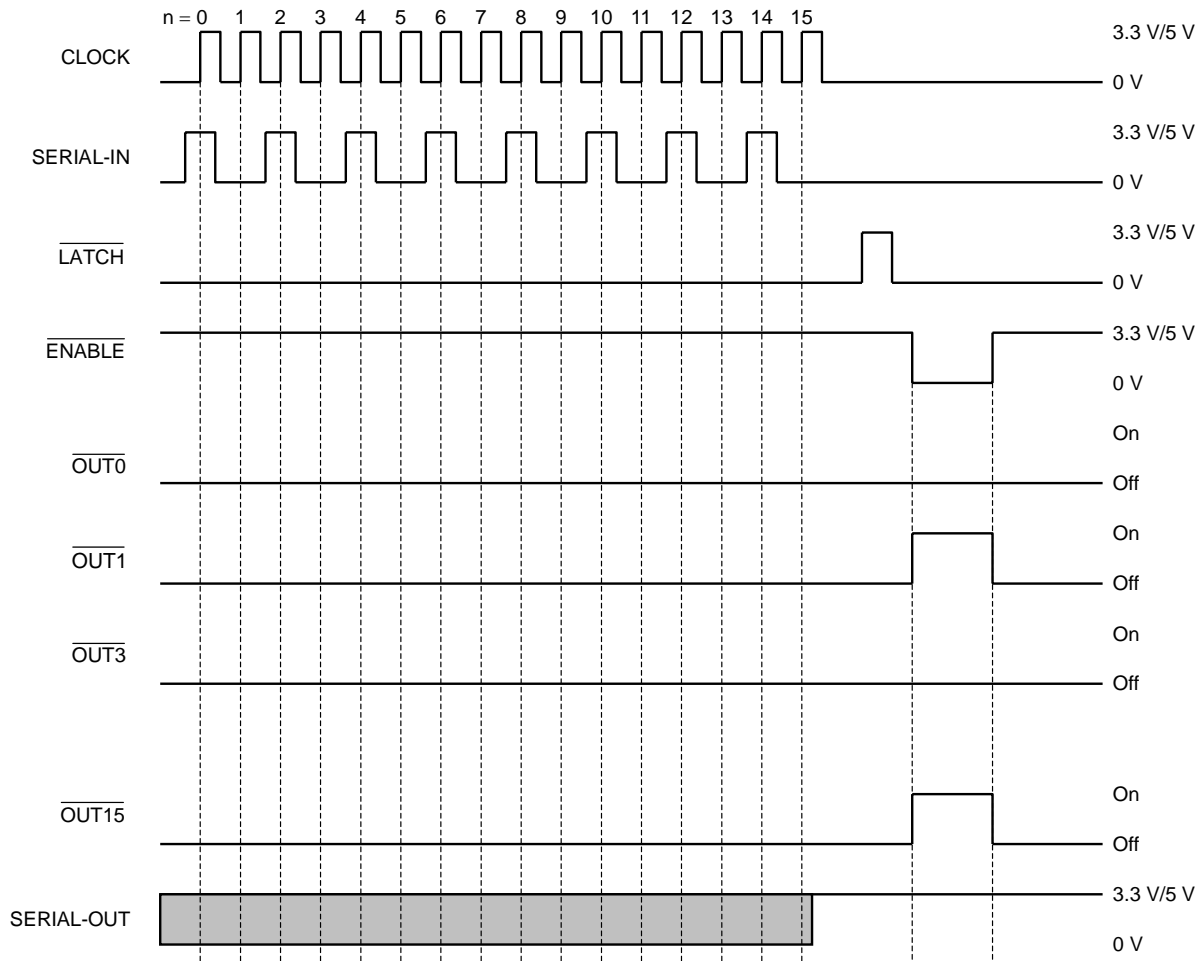
Truth Table

CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL-IN	$\overline{\text{OUT0}} \dots \overline{\text{OUT7}} \dots \overline{\text{OUT15}}$	SERIAL-OUT
\uparrow	H	L	D_n	$D_n \dots D_{n-7} \dots D_{n-15}$	D_{n-15}
\uparrow	L	L	D_{n+1}	No change	D_{n-14}
\uparrow	H	L	D_{n+2}	$D_{n+2} \dots D_{n-5} \dots D_{n-13}$	D_{n-13}
\downarrow	X	L	D_{n+3}	$D_{n+2} \dots D_{n-5} \dots D_{n-13}$	D_{n-13}
\downarrow	X	H	D_{n+3}	OFF	D_{n-13}

Note 1: $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ = On when $D_n = H$; $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ = Off when $D_n = L$.

In order to ensure that the level of the power supply voltage is correct, an external resistor must be connected between R-EXT and GND.

Timing Diagram



Warning: Latch circuit is leveled-latch circuit. Be careful because it is not triggered-latch circuit.

Note 2: The latches circuit holds data by pulling the $\overline{\text{LATCH}}$ terminal Low.

And, when $\overline{\text{LATCH}}$ terminal is a High level, latch circuit doesn't hold data, and it passes from the input to the output.

When $\overline{\text{ENABLE}}$ terminal is a Low level, output terminal $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ respond to the data, and on and off does.

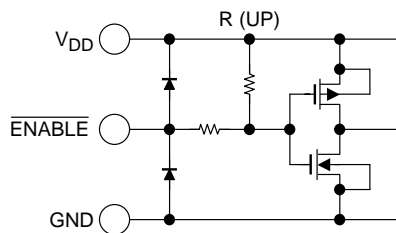
And, when $\overline{\text{ENABLE}}$ terminal is a High level, it offs with the output terminal regardless of the data.

Terminal Description

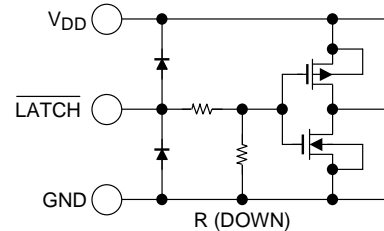
Pin No.	Pin Name	Function
1	GND	GND terminal for control logic
2	SERIAL-IN	Input terminal for serial data for data shift register
3	CLOCK	Input terminal for clock for data shift on rising edge
4	$\overline{\text{LATCH}}$	Input terminal for data strobe When the $\overline{\text{LATCH}}$ input is driven High, data is not latched. When it is pulled Low, data is latched.
5 to 20	$\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$	Constant-current output terminals
21	$\overline{\text{ENABLE}}$	Input terminal for output enable. All outputs ($\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$) are turned off, when the $\overline{\text{ENABLE}}$ terminal is driven High. And are turned on, when the terminal is driven Low.
22	SERIAL-OUT	Output terminal for serial data input on SERIAL-IN terminal
23	R-EXT	Input terminal used to connect an external resistor. This regulated the output current.
24	V_{DD}	3.3-V/5-V supply voltage terminal

Equivalent Circuits for Inputs and Outputs

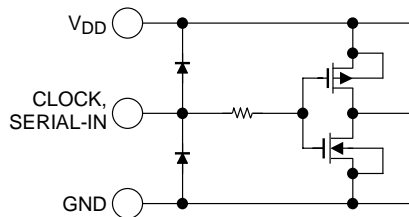
1. $\overline{\text{ENABLE}}$ terminal



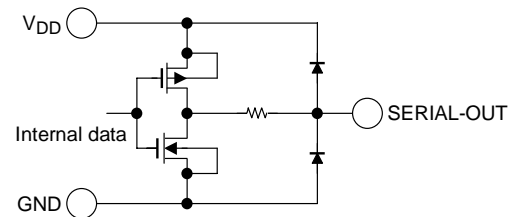
2. $\overline{\text{LATCH}}$ terminal



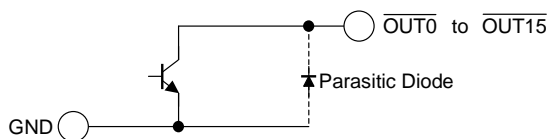
3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



5. $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ terminals



Maximum Ratings (T_{opr} = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage		V _{DD}	6	V
Input voltage		V _{IN}	-0.2 to V _{DD} + 0.2	V
Output current		I _{OUT}	+90	mA/ch
Output voltage		V _{OUT}	-0.2 to 17	V
Power dissipation (Note 3)	ANG-type (when not mounted)	P _{d1}	1.25	W
	ANG-type (on PCB)		1.78	
	AFG-type (when not mounted)	P _{d2}	0.83	
	AFG-type (on PCB)		1.00	
Thermal resistance (Note 3)	ANG-type (when not mounted)	R _{th(j-a) 1}	104	°C/W
	ANG-type (on PCB)		70	
	AFG-type (when not mounted)	R _{th(j-a) 2}	140	
	AFG-type (on PCB)		120	
Operating temperature		T _{opr}	-40 to 85	°C
Storage temperature		T _{stg}	-55 to 150	°C

Note 3: ANG-Type: Powers dissipation is derated by 14.28 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.

AFG-Type: Powers dissipation is derated by 6.67 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.

With device mounted on glass-epoxy PCB of less than 40% Cu and of dimensions 50 mm × 50 mm × 1.6 mm.

Recommended Operating Conditions (T_{opr} = -40°C to 85°C unless otherwise specified)

Characteristics	Symbol	Conditions	Min	Typ.	Max	Unit
Supply voltage	V _{DD}	—	3	—	5.5	V
Output voltage	V _{OUT}	—	—	0.7	4	V
Output current	I _{OUT}	Each DC 1 circuit	2	—	80	mA/ch
	I _{OH}	SERIAL-OUT	—	—	-1	mA
	I _{OL}	SERIAL-OUT	—	—	1	
Input voltage	V _{IH}	—	0.7 × V _{DD}	—	V _{DD} + 0.15	V
	V _{IL}		-0.15	—	0.3 × V _{DD}	
Clock frequency	f _{CLK}	Cascade connected	—	—	20	MHz
$\overline{\text{LATCH}}$ pulse width	t _{wLAT}		50	—	—	ns
CLOCK pulse width	t _{wCLK}	—	25	—	—	ns
ENABLE pulse width (Note 4)	t _{wENA}	Upper I _{OUT} = 20 mA	2000	—	—	ns
		Lower I _{OUT} = 20 mA	3000	—	—	
Set-up time for CLOCK terminal	t _{SETUP1}	—	10	—	—	ns
Hold time for CLOCK terminal	t _{HOLD}		10	—	—	ns
Set-up time for $\overline{\text{LATCH}}$ terminal	t _{SETUP2}		50	—	—	ns

Note 4: When the pulse of the Low level is inputted to the $\overline{\text{ENABLE}}$ terminal held in the High level.

Electrical Characteristics ($T_{opr} = 25^{\circ}\text{C}$, $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ unless otherwise specified)

Characteristics	Symbol	Conditions		Min	Typ.	Max	Unit	
Supply voltage	V_{DD}	Normal operation		3.0	—	5.5	V	
Output current	I_{OUT1}	$V_{OUT} = 0.4\text{ V}$, $V_{DD} = 3.3\text{ V}$	$R_{EXT} = 490\ \Omega$	31.96	36.20	40.54	mA	
	I_{OUT2}	$V_{OUT} = 0.4\text{ V}$, $V_{DD} = 5\text{ V}$		31.59	35.90	40.20		
	I_{OUT3}	$V_{OUT} = 0.7\text{ V}$, $V_{DD} = 3.3\text{ V}$	$R_{EXT} = 250\ \Omega$	63.63	72.30	80.97		
	I_{OUT4}	$V_{OUT} = 0.7\text{ V}$, $V_{DD} = 5\text{ V}$		62.75	71.30	79.95		
Output current error between bits	ΔI_{OUT1}	$V_{OUT} \geq 0.4\text{ V}$, All outputs ON	$R_{EXT} = 490\ \Omega$	—	± 1	± 4	%	
	ΔI_{OUT2}	$V_{OUT} \geq 0.4\text{ V}$, All outputs ON	$R_{EXT} = 250\ \Omega$					
Output leakage current input voltage	I_{OZ}	$V_{OUT} = 15.0\text{ V}$		—	—	1	μA	
Input voltage	V_{IN}	—		$0.7 V_{DD}$	—	V_{DD}	V	
		—		GND	—	$0.3 V_{DD}$		
SOUT terminal voltage	V_{OL}	$I_{OL} = 1.0\text{ mA}$, $V_{DD} = 3.3\text{ V}$		—	—	0.3	V	
		$I_{OL} = 1.0\text{ mA}$, $V_{DD} = 5\text{ V}$		—	—	0.3		
	V_{OH}	$I_{OH} = -1.0\text{ mA}$, $V_{DD} = 3.3\text{ V}$		3	—	—		
		$I_{OH} = 1.0\text{ mA}$, $V_{DD} = 5\text{ V}$		4.7	—	—		
Output current Supply voltage Regulation	$\%V_{DD}$	When V_{DD} is changed 3 V to 5.5 V		—	-1	-5	%	
Pull-up resistor	$R_{(Up)}$	$\overline{\text{ENABLE}}$ terminal		115	230	460	k Ω	
Pull-down resistor	$R_{(Down)}$	$\overline{\text{LATCH}}$ terminal						
Supply current	$I_{DD}(\text{OFF})1$	$V_{OUT} = 15.0\text{ V}$	$R_{EXT} = \text{OPEN}$	—	0.1	0.5	mA	
	$I_{DD}(\text{OFF})2$	$V_{OUT} = 15.0\text{ V}$, All outputs OFF	$R_{EXT} = 490\ \Omega$	1	3.5	5		
	$I_{DD}(\text{OFF})3$	$V_{OUT} = 15.0\text{ V}$, All outputs OFF	$R_{EXT} = 250\ \Omega$	4	6	9		
	$I_{DD}(\text{ON})1$	$V_{OUT} = 0.7\text{ V}$, All outputs ON		$R_{EXT} = 490\ \Omega$	—	9		15
		Same as the above, $T_{opr} = -40^{\circ}\text{C}$			—	—		20
	$I_{DD}(\text{ON})2$	$V_{OUT} = 0.7\text{ V}$, All outputs ON		$R_{EXT} = 250\ \Omega$	—	18		25
Same as the above, $T_{opr} = -40^{\circ}\text{C}$			—	—	40			

Switching Characteristics ($T_{opr} = 25^{\circ}\text{C}$ unless otherwise specified)

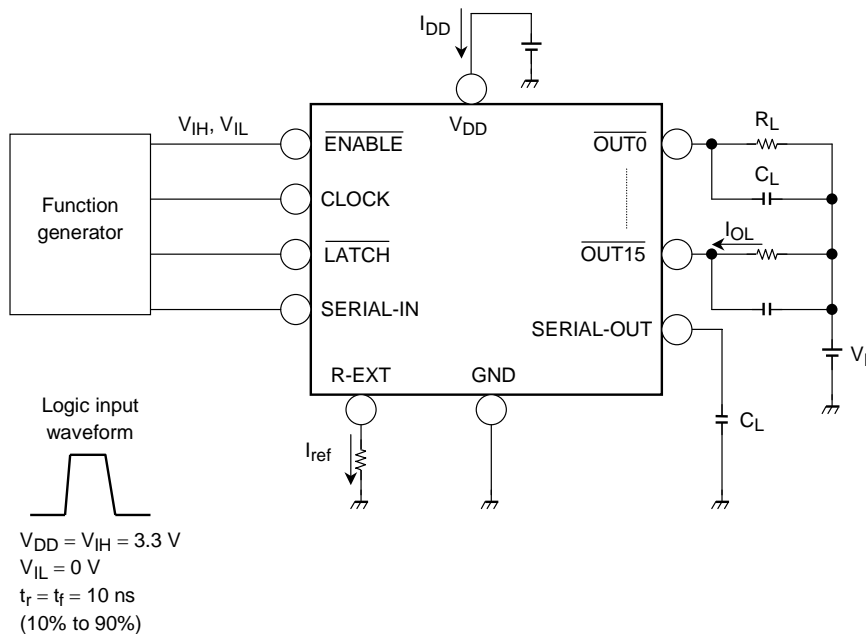
Characteristics	Symbol	Conditions	Min	Typ.	Max	Unit
Propagation delay	t_{pLH1}	$\text{CLK} - \overline{\text{OUTn}}$, $\overline{\text{LATCH}} = \text{"H"}$, $\overline{\text{ENABLE}} = \text{"L"}$	—	150	300	ns
	t_{pLH2}	$\overline{\text{LATCH}} - \overline{\text{OUTn}}$, $\overline{\text{ENABLE}} = \text{"L"}$	—	140	300	
	t_{pLH3}	$\overline{\text{ENABLE}} - \overline{\text{OUTn}}$, $\overline{\text{LATCH}} = \text{"H"}$	—	140	300	
	t_{pLH}	CLK-SERIAL OUT	3	6	—	
	t_{pHL1}	$\text{CLK} - \text{OUTn}$, $\overline{\text{LATCH}} = \text{"H"}$, $\overline{\text{ENABLE}} = \text{"L"}$	—	170	340	
	t_{pHL2}	$\overline{\text{LATCH}} - \text{OUTn}$, $\overline{\text{ENABLE}} = \text{"L"}$	—	170	340	
	t_{pHL3}	$\overline{\text{ENABLE}} - \text{OUTn}$, $\overline{\text{LATCH}} = \text{"H"}$	—	170	340	
	t_{pLH}	CLK-SERIAL OUT	4	7	—	
Output rise time	t_{or}	10 to 90% of voltage waveform	40	85	150	ns
Output fall time	t_{of}	90 to 10% of voltage waveform	40	70	150	ns
Maximum CLOCK rise time	t_r	When not on PCB (Note 5)	—	—	5	μs
Maximum CLOCK fall time	t_f		—	—	5	μs

Conditions: (Refer to test circuit.)

$T_{opr} = 25^{\circ}\text{C}$, $V_{DD} = V_{IH} = 3.3\text{ V}$ and 5 V , $V_{OUT} = 0.7\text{ V}$, $V_{IL} = 0\text{ V}$, $R_{EXT} = 490\ \Omega$,
 $V_L = 3.0\text{ V}$, $R_L = 60\ \Omega$, $C_L = 10.5\text{ pF}$

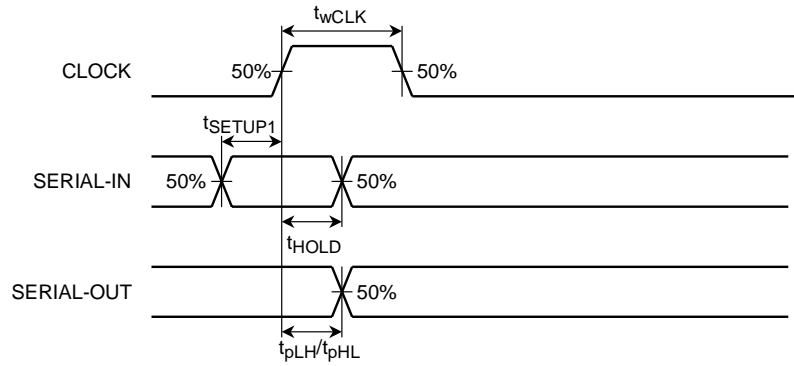
Note 5: If the device is connected in a cascade and t_r/t_f for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.

Test Circuit

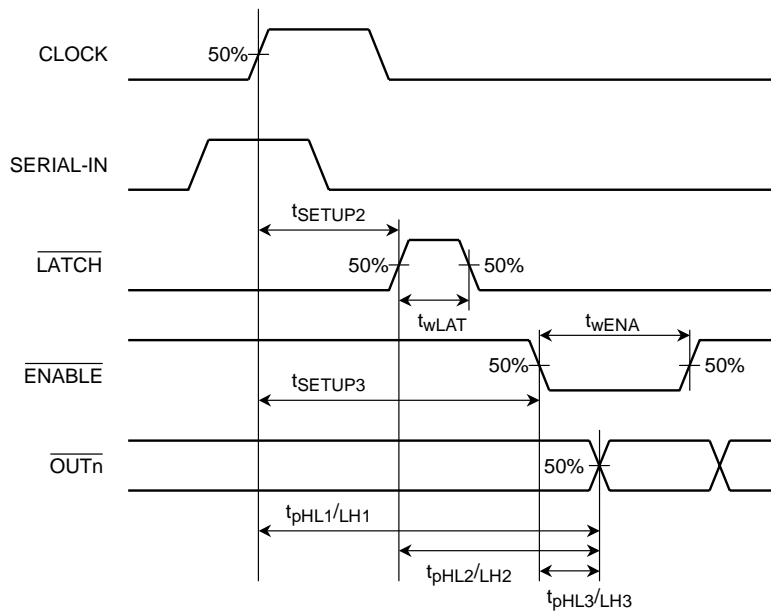


Timing Waveforms

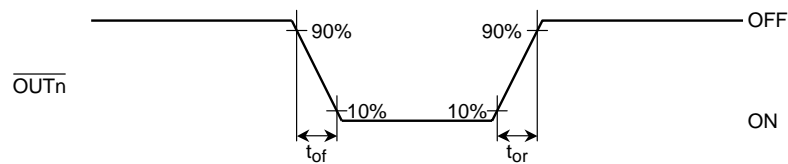
1. CLOCK, SERIAL-IN, SERIAL-OUT



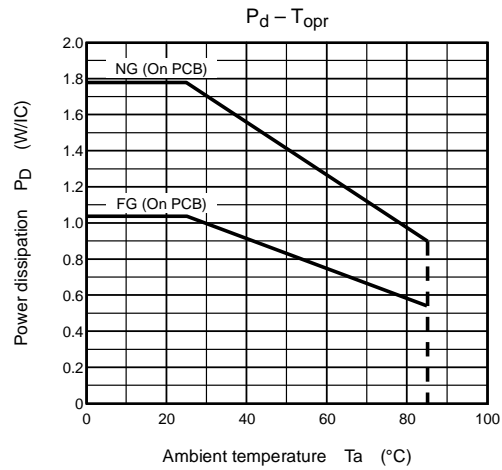
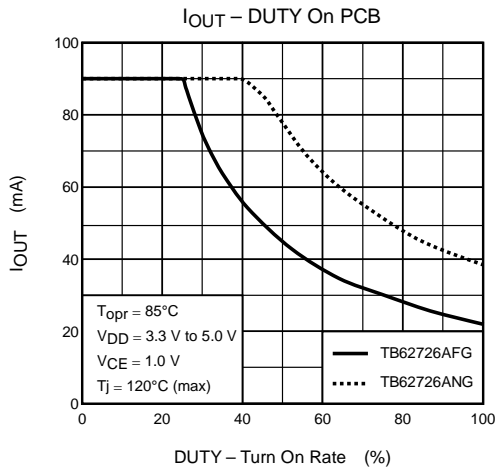
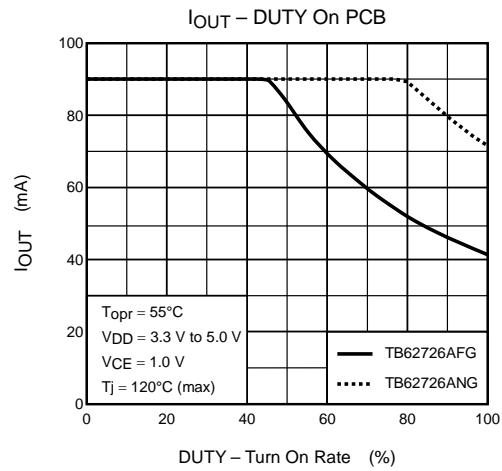
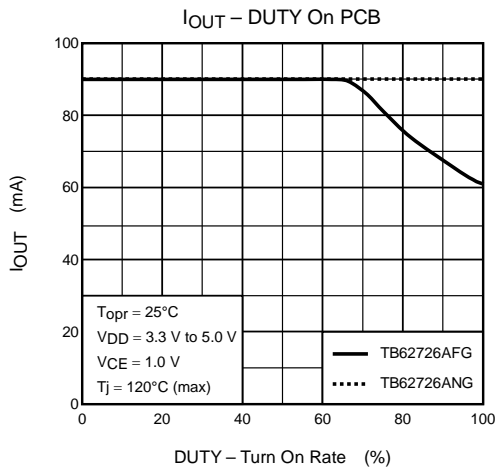
2. CLOCK, SERIAL-IN, LATCH, ENABLE, OUTn



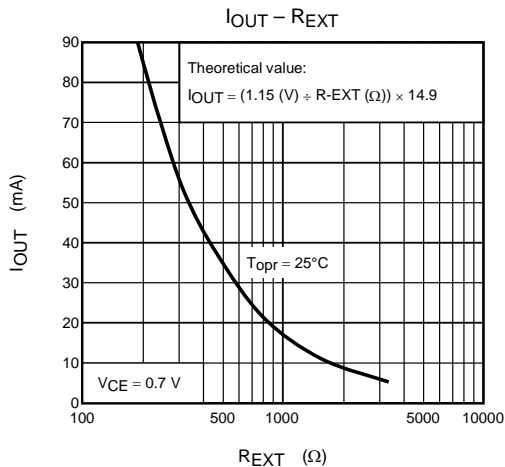
3. \overline{OUTn}



Output Current – Duty (LEDS turn-on rate)



Output Current – R_{EXT} Resistor

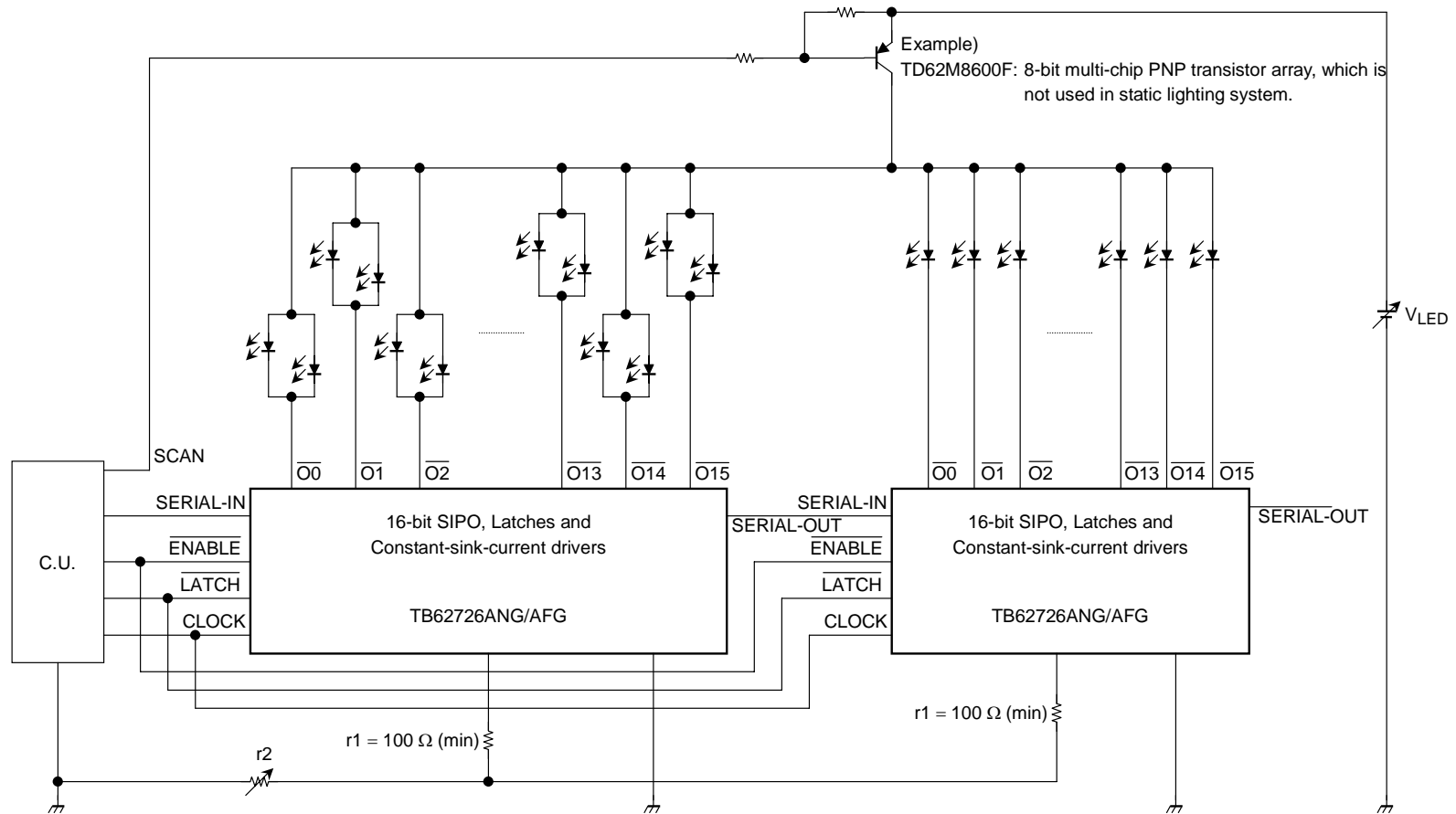


Application Circuit (example 1): The general composition in static lighting of LED.

More than $V_{LED} (V) \geq V_f (\text{total max}) + 0.7$ is recommended with the following application circuit with the LED power supply V_{LED} .

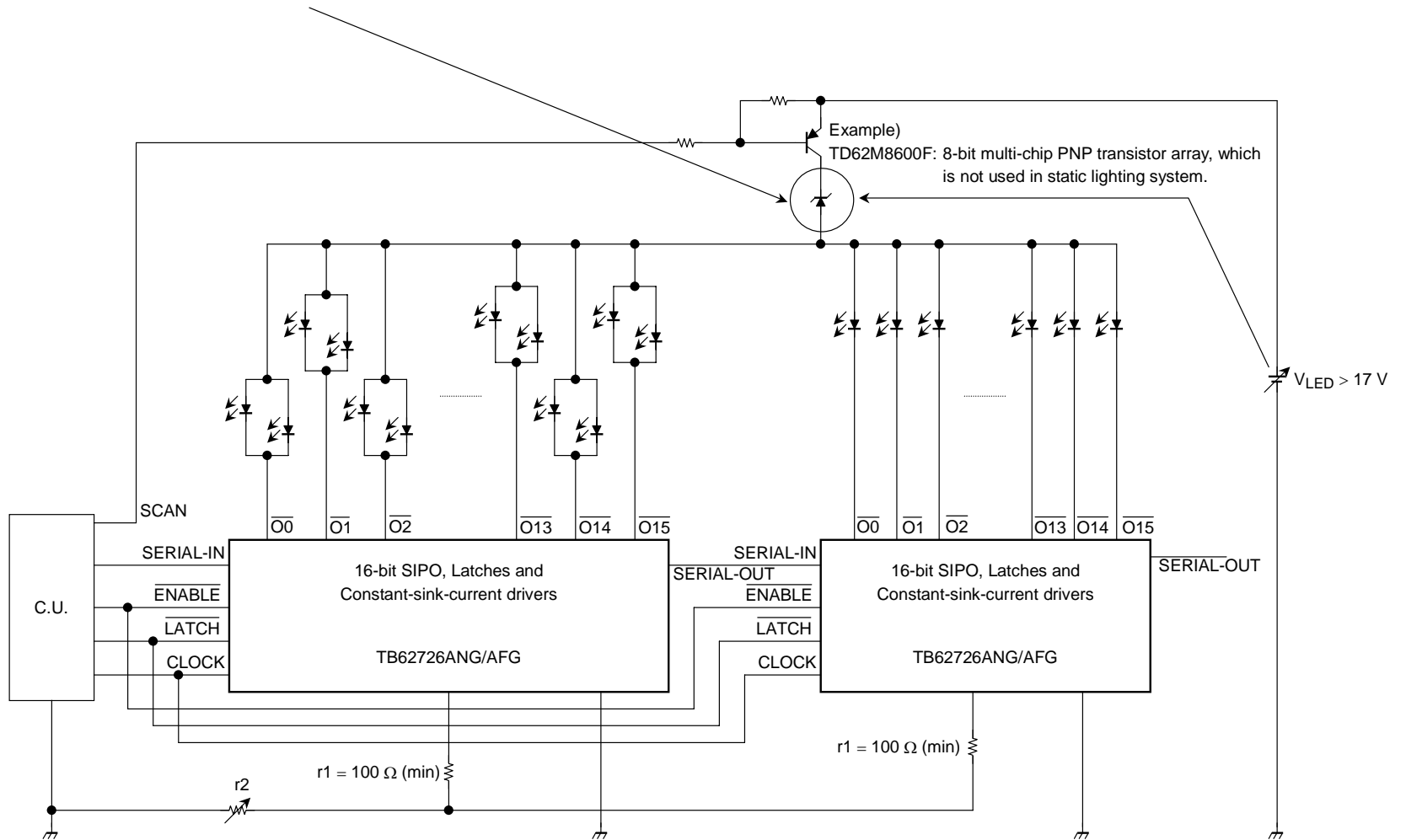
r1: The setup resistance for the setup of output current of every IC.

r2: The variable resistance for the brightness control of every LED module.



Application Circuit (example 2): When the condition of VLED is $V_{LED} > 17\text{ V}$

The unnecessary voltage is one effective technique as to making the voltage descend with the zenor diode.



Application Circuit (example 3): When the condition of VLED is $V_f + 0.7 < V_{LED} < 17 V$

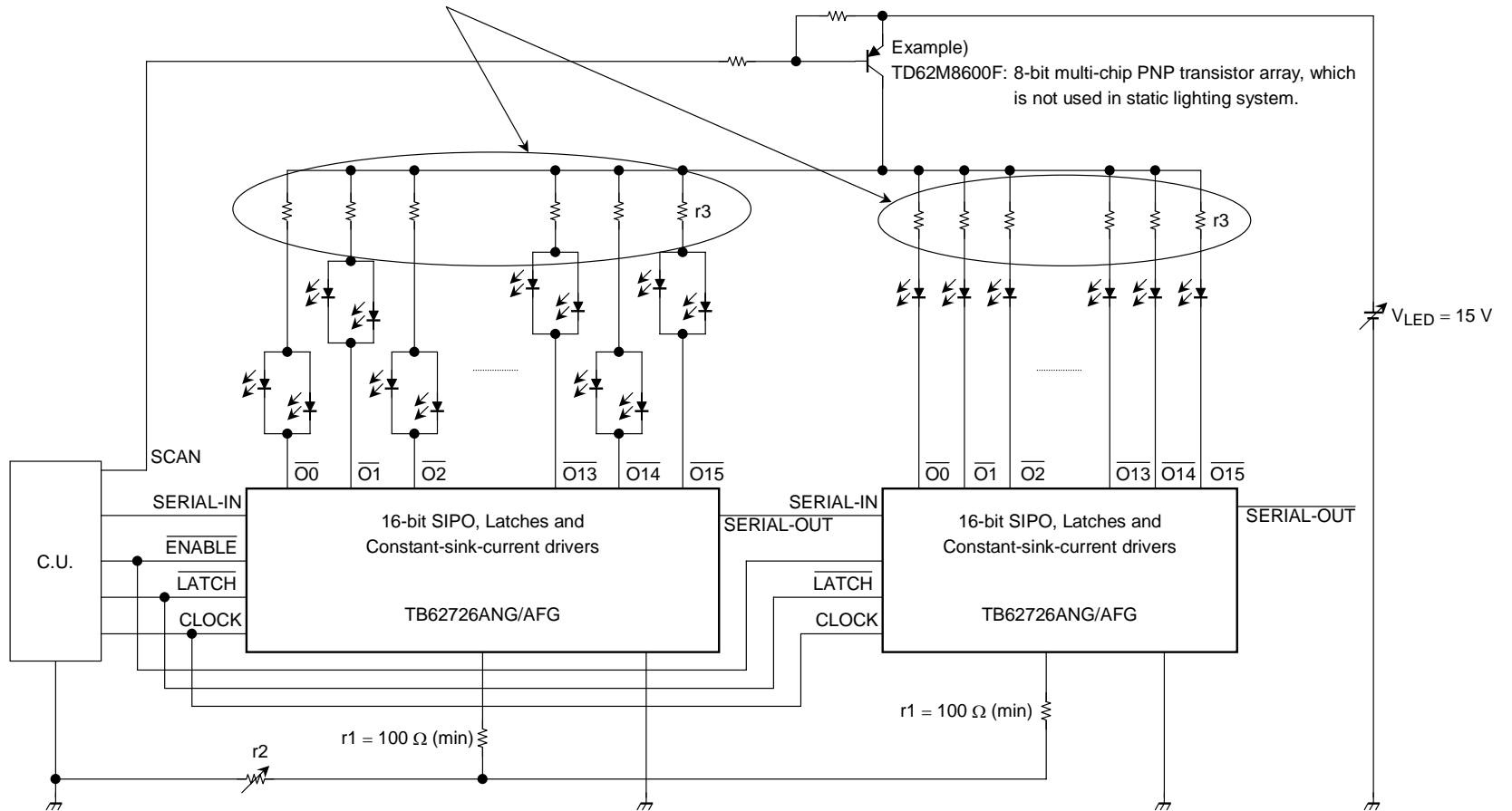
$V_{OUT} = V_{LED} - V_f = 0.7$ to $1.0 V$ is the most suitable for V_{OUT} .

Surplus V_{OUT} causes an IC fever and the useless consumption electric power.

It is the one way of being effective to build in the $r3$ in this problem.

$r3$ can make a calculation to the formula $r3 \Omega = \text{surplus } V_{OUT} / I_{OUT}$.

Though the resistance parts increase, the fixed constant current performance is kept



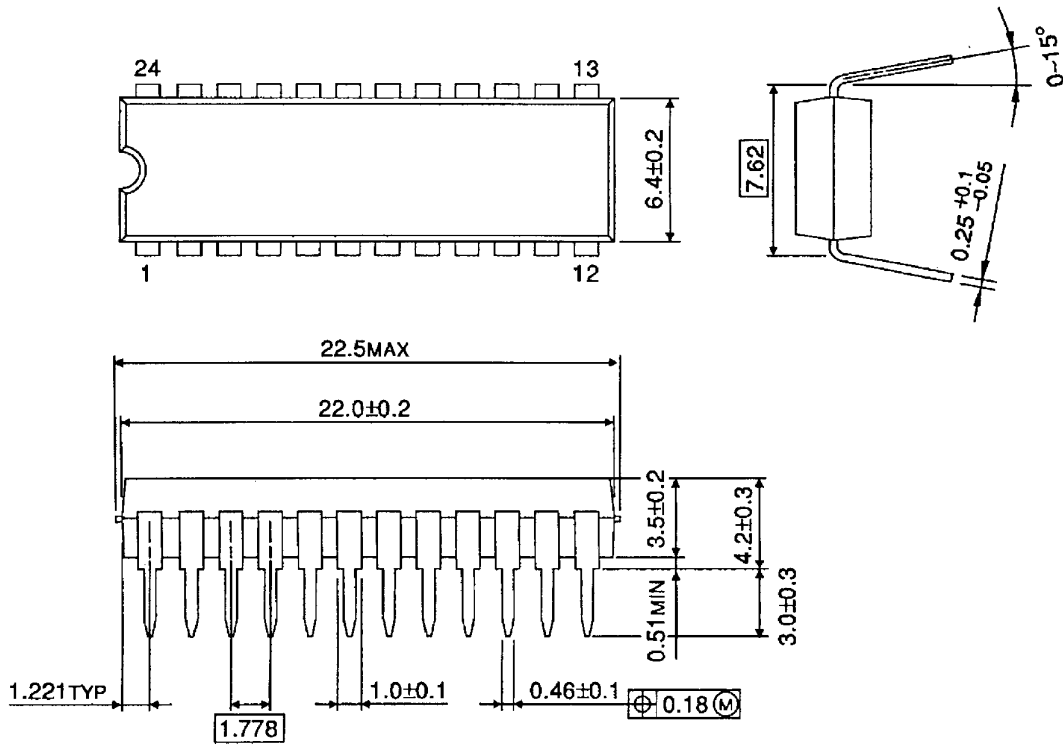
Notes

- Operation may become unstable due to the electromagnetic interference caused by the wiring and other phenomena.
To counter this, it is recommended that the IC be situated as close as possible to the LED module.
If overvoltage is caused by inductance between the LED and the output terminals, both the LED and the terminals may suffer damage as a result.
- There is only one GND terminal on this device when the inductance in the GND line and the resistor are large, the device may malfunction due to the GND noise when output switchings by the circuit board pattern and wiring.
To achieve stable operation, it is necessary to connect a resistor between the REXT terminal and the GND line.
Fluctuation in the output waveform is likely to occur when the GND line is unstable or when a capacitor (of more than 50 pF) is used.
Therefore, take care when designing the circuit board pattern layout and the wiring from the controller.
- This application circuit is a reference example and is not guaranteed to work in all conditions.
Be sure to check the operation of your circuits.
- This device does not include protection circuits for overvoltage, overcurrent or overtemperature.
If protection is necessary, it must be incorporated into the control circuitry.
- The device is likely to be destroyed if a short-circuit occurs between either of the power supply pins and any of the output terminals when designing circuits, pay special attention to the positions of the output terminals and the power supply terminals (VDD and VLED), and to the design of the GND line.

Package Dimensions

SDIP24-P-300-1.78

Unit : mm

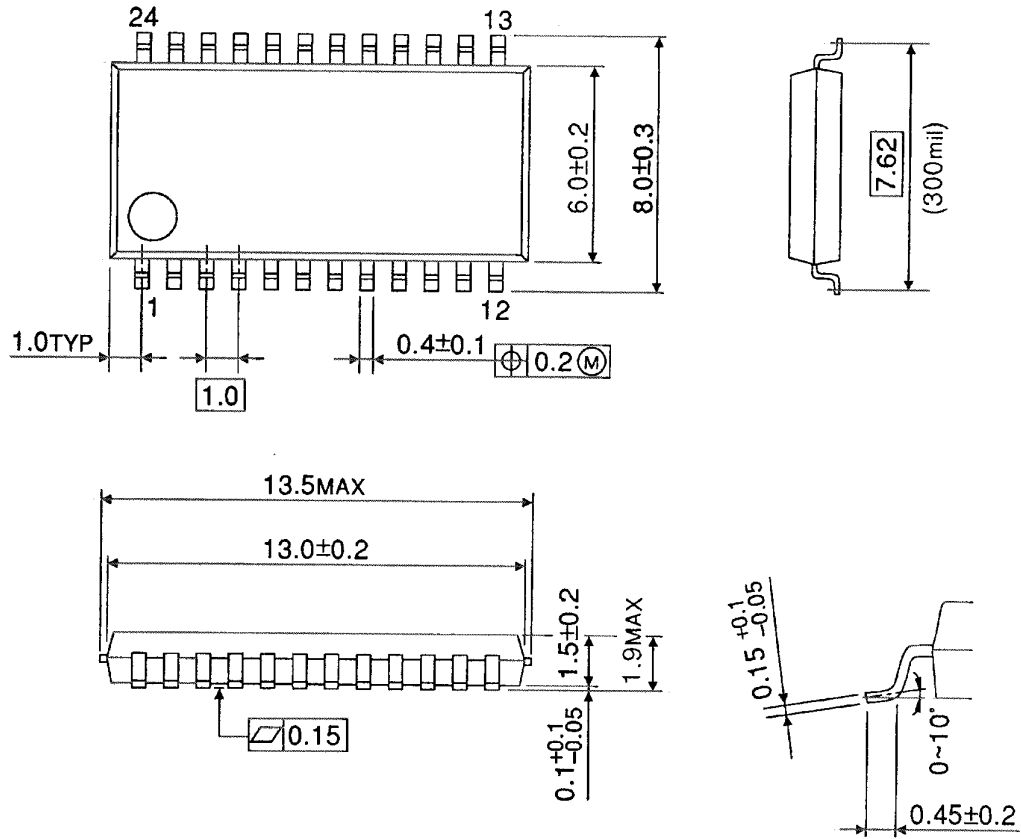


Weight: 1.22 g (typ.)

Package Dimensions

SSOP24-P-300-1.00B

Unit : mm



Weight: 0.32 g (typ.)

Notes on Contents**1. Block Diagrams**

Some functional blocks, circuits, or constants may be omitted or simplified in the block diagram for explanatory purposes.

2. Maximum Ratings

The absolute maximum ratings of a semiconductor device are a set of specified parameter values that must not be exceeded during operation, even for an instant.

If any of these ratings are exceeded during operation, the electrical characteristics of the device may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed.

Moreover, any exceeding of the ratings during operation may cause breakdown, damage and/or degradation in other equipment. Applications using the device should be designed so that no maximum rating will ever be exceeded under any operating conditions.

Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

3. Recommended operating conditions

The values of the conditions are applied within the range of the operating temperature and not guaranteed.

4. Test Circuits

Components in test circuits are used only to obtain and confirm device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure in application equipment.

5. Graphics characteristics

Graphics characteristics are reference ones and not guaranteed.

6. Timing Charts

Timing charts may be simplified for explanatory purposes.

7. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

8. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially in the phase of mass production design.

In furnishing these examples of application circuits, Toshiba does not grant the use of any industrial property rights.

Handling of the IC

Ensure that the product is installed correctly to prevent breakdown, damage and/or degradation in the product or equipment.

About solderability, following conditions were confirmed

- Solderability
 - (1) Use of Sn-37Pb solder Bath
 - solder bath temperature = 230°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux
 - (2) Use of Sn-3.0Ag-0.5Cu solder Bath
 - solder bath temperature = 245°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux

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030619EBA

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